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Application Notes for  
Surface Mount Assembly of Amkor's  
Dual Row *MicroLeadFrame*® (MLF) Packages

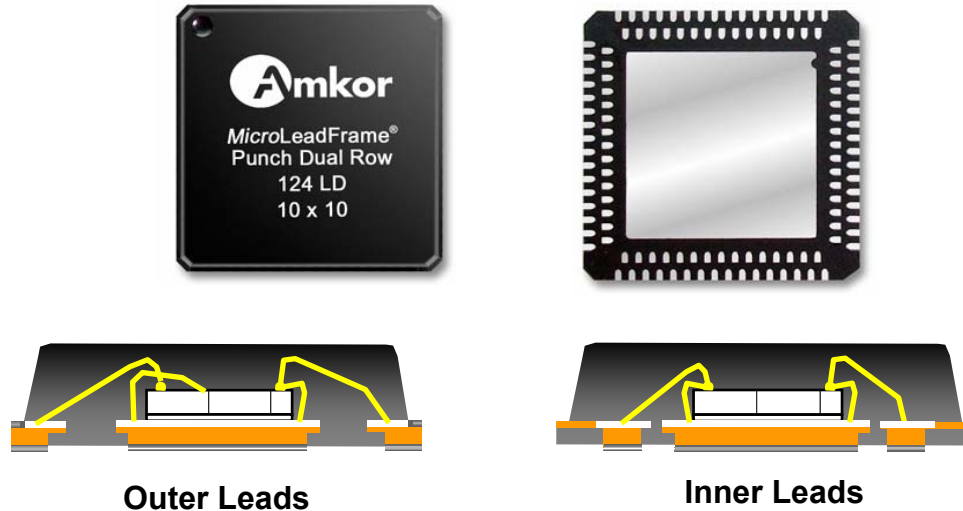


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## 1. Introduction

The Dual Row *MicroLeadFrame*® package (MLF) is a near CSP plastic encapsulated package with a copper leadframe substrate. This is an extension to the standard single row *MicroLeadFrame*® (MLF) leadless package where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB with an additional row of leads on the package. Amkor's ePad technology enhances the thermal and electrical properties of the package. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds and electrical connections through conductive die attach material. The design of the *MicroLeadFrame*® package also allows for flexibility. Its enhanced electrical performance enables the standard 2 GHz operating frequency to be increased up to 10 GHz with some design considerations.



**Figure 1. Dual Row MLF Package Photo and Cross Section Drawings**

The Dual row design utilizes an interstitial lead design that results in a staggered lead arrangement. External leads are a full lead design similar to the single row version. The inner row is offset 0.65 mm or 0.75 mm, depending on lead pitch, which results in a compact design that maximizes die size while not exceeding SMT capability of a typical 0.50mm pitch SMT process.

## 2. Surface Mount Considerations for Dual Row MLF Package

In order to perform at peak, special considerations are needed to properly design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed pad on the package needs to be soldered to the board using a corresponding thermal pad on the board. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region. Clearance between the inner row leads and the thermal pad for vias to route the inner row signals are required. The amount of clearance required depends on the application. The PCB footprint design needs to be considered from dimensional tolerances due to package, PCB, and assembly.

A number of factors may have a significant effect on mounting MLF package on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. This applications note provides the guidelines for this purpose. It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort maybe needed to optimize the process as per user's surface mount practices and requirements.

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### 3. PCB Design Guidelines

This application note will address both package level and board level routing constraints in describing the philosophy behind the recommended land patterns.

#### 3.1. Dual Row Interstitial package dimensions

Figure 2 shows the relevant dimensions required to develop a land pattern for dual row MLF packages. Typical values for selected packages are also listed in Table 1. For this figure and subsequent land pattern figures, it is assumed the package is square for simplicity. Lead dimensioning is similar to the single row MLF, but with the addition of a basic row pitch dimension ( $eR$ ). Actual package outlines do not describe an S2 or S3 dimension, but instead describe the inner leads in terms of positional tolerances about basic dimensions at MMC. To develop a land pattern, values for S2 and S3 must be calculated.

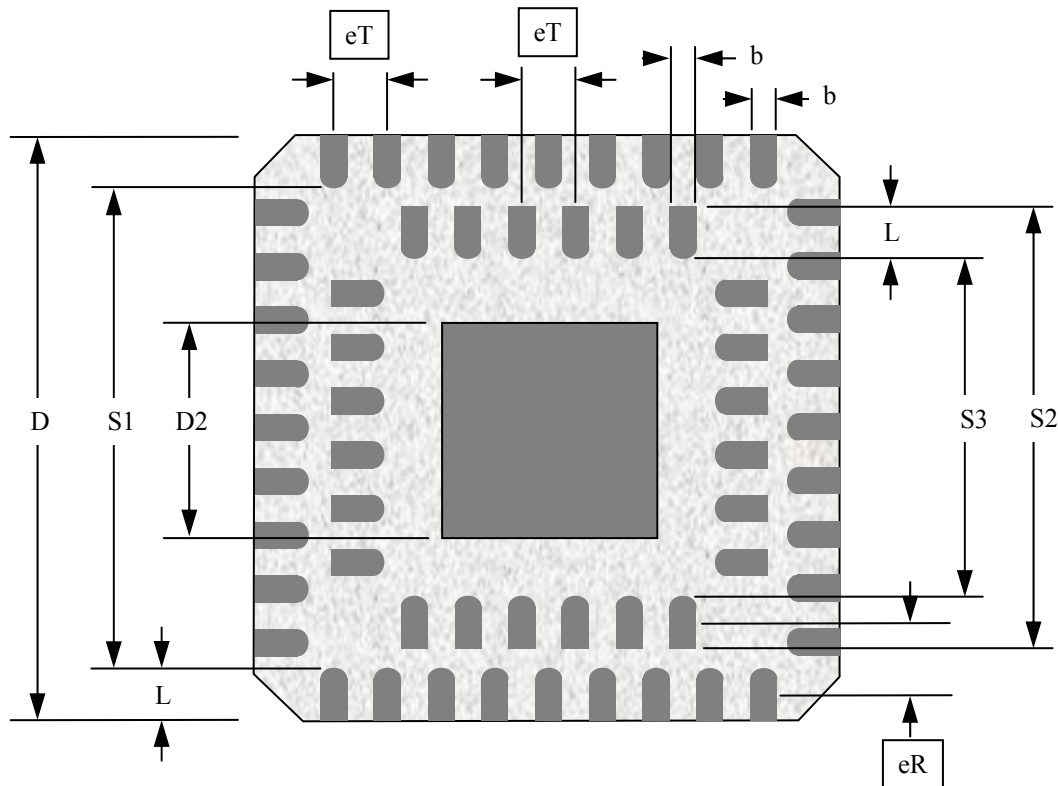
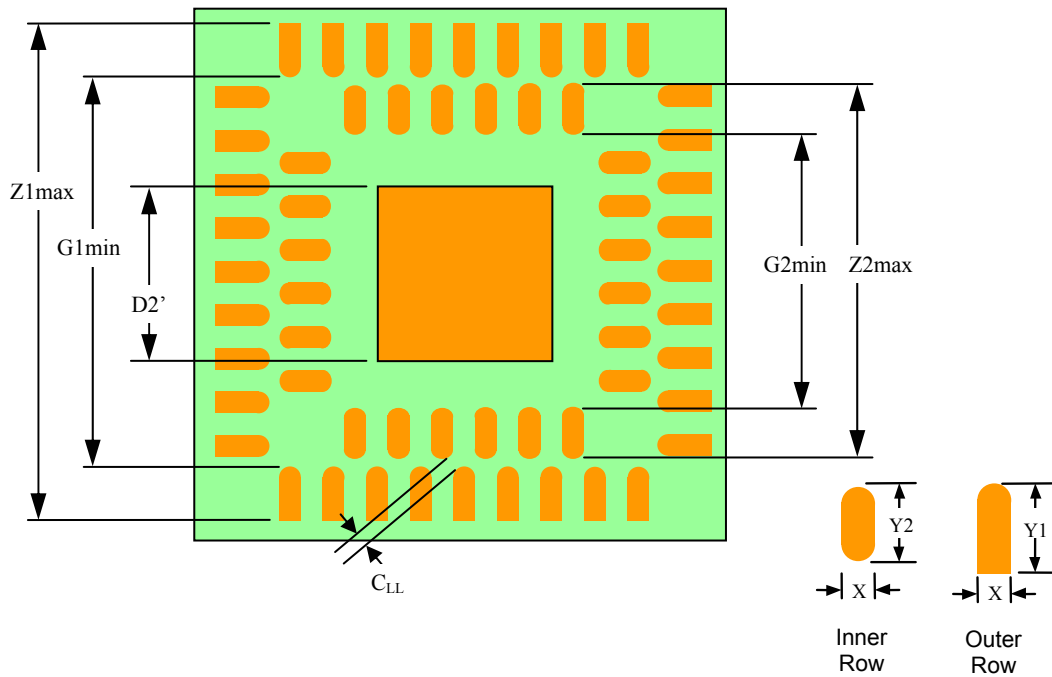


Figure 2. Dual Row MLF component dimensions needed for PCB land pattern design.

#### 3.2. PCB Land Pattern

The methodology developed by IPC and documented in IPC-7351 (formerly IPC-SM-782) and normally used for standard single row MLF cannot completely be used for dual row MLF designs. Main reason is due to the multi-row nature of the package that has more in common with BGA land pattern design than with perimeter leadframe packages. Application of the standard IPC design methodology would actually result in overlap of the inner and outer row leads and lead to an unmanufacturable board design. It is also desirable to design the land pattern to maximize the self centering capability of the package without sacrificing solder joint reliability. Thus a different approach was taken to arrive at the basic land pattern for dual row MLF.

Figure 3 below shows the dimensions and symbols of the land pattern that is to be determined. All dimensions calculated follow the same IPC-7351 convention of describing the land pattern at MMC condition. For convenience, most land pattern dimensions are described in a “Body Size – XXX” format.



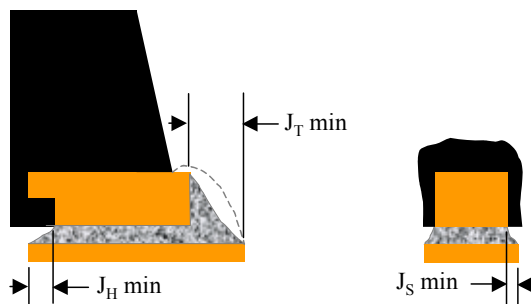
**Figure 3. PCB Land Pattern Dimensions to be Determined.**

Common Tolerances used for all calculations are:

- Board fabrication tolerance (F) = 0.10mm (±0.05mm, typical capability of board fabricators)
- Component placement tolerance (P) = 0.10mm (±0.05mm, typical capability of P&P machines)
- Component length tolerance ( $L_{Tot} = C_L$ ) = 0.20mm (from package outline drawing “aaa”, 0.10mm profile tolerance)
- Minimum Land – Land Spacing ( $C_{LL}$ ) = 0.20mm (compatible with current 0.50mm pitch SMT processes)

The minimum values for solder joint fillets, defined in Figure 4, used to calculate the land pattern dimensions are:

- Minimum Toe Fillet ( $J_T$ ) = 0.10mm
- Minimum Heel Fillet ( $J_H$ ) = 0.05mm
- Minimum Side Fillet ( $J_S$ ) = 0.00mm



**Figure 4: Definition of toe, heel, and side fillets.**

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### 3.3. Land Pattern Dimensions for Leads

#### 3.3.1. 0.500 mm pitch applications

First, the land width (X) for both inner and outer rows is needed. Based on history of single row MLF, a lead width (X) of 0.280mm was chosen for 0.500mm pitch. Outer row land pattern dimension  $Z1_{Max}$  is calculated using standard IPC methodology and expressed in terms of nominal body size dimension:

$$Z1_{Max} = D_{Min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$
$$D_{Min} = BODYSIZE - \frac{C_L}{2}$$
$$Z1_{Max} = BODYSIZE + 0.340 \text{ mm}$$

For  $G1_{Min}$  and  $Z2_{Max}$  values, a minimum clearance of 0.200 mm between inner and outer leads must be maintained. For a 0.280 mm lead width and 0.650 mm row pitch, a spacing of 0.130 mm between the inner and outer row leads must be maintained (i.e.  $\frac{1}{2}(G1_{Min} - Z2_{Max}) \geq 0.130 \text{ mm}$ ). The nominal distance between package leads is 0.250 mm. Thus the extra 0.120 mm space for toe and heel fillets must be partitioned between the inner and outer leads. Because the toe fillet is more important to solder joint reliability, a design rule of  $J_T \geq 2 J_H$  is used (i.e.  $J_T = 0.080 \text{ mm}$ ,  $J_H = 0.040 \text{ mm}$ ). This results in the following:

$$G1_{Min} = BODYSIZE - 0.880 \text{ mm}$$
$$Z2_{Max} = BODYSIZE - 1.140 \text{ mm}$$

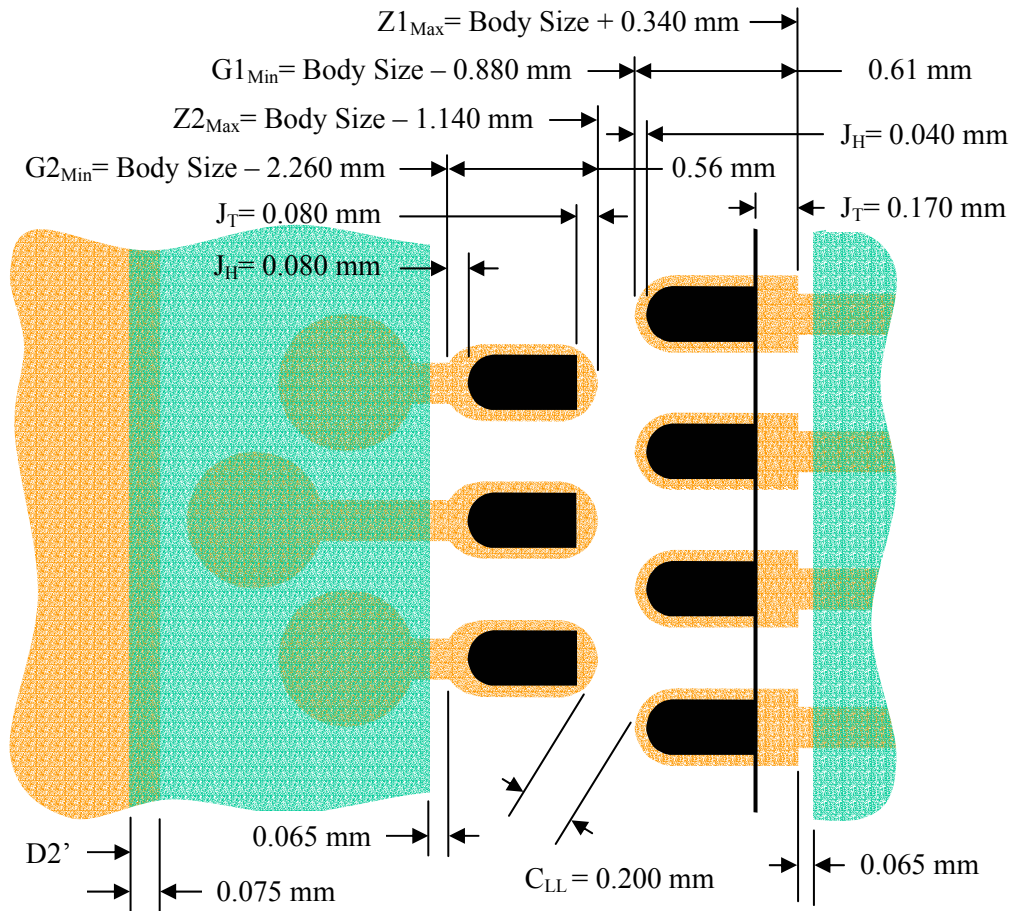
For  $G2_{Min}$  dimension, the heel fillet is limited to conserve space for inner row vias between the leads and the thermal pad. A value similar to the toe fillet is chosen,  $J_H = 0.080 \text{ mm}$ . This results in the following:

$$G2_{Min} = BODYSIZE - 2.260 \text{ mm}$$

The individual lead dimensions derived from these values are:

Outer row leads: 0.280 x 0.610 mm  
Inner row Lead: 0.280 x 0.560 mm

Figure 5 shows the land pattern in graphical format.



**Figure 5: Land Pattern for 0.50mm pitch Dual Row MLF.**

### 3.3.2. 0.650 mm pitch applications

For 0.650 mm pitch packages, the same land length and width used for 0.500 mm pitch applications is recommended. This allows routing of all signals on a single layer by routing the inner row traces between outer row leads. This will require the use of 0.100 mm width traces to maintain required solder mask coverage. By routing all signals on a single layer, low cost 2-layer boards are possible. This also maximizes the thermal pad size. See figure 6 for a typical design example.

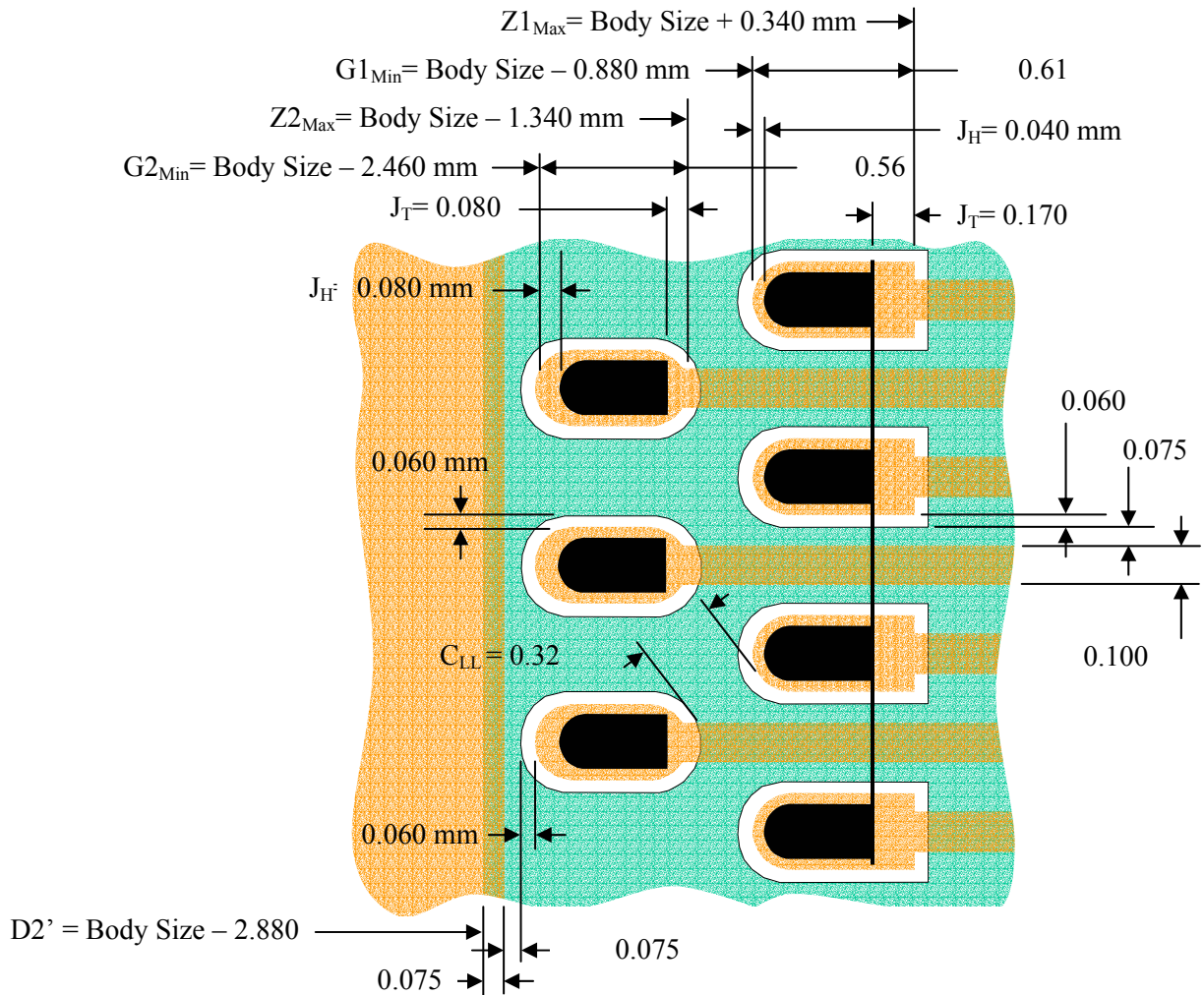
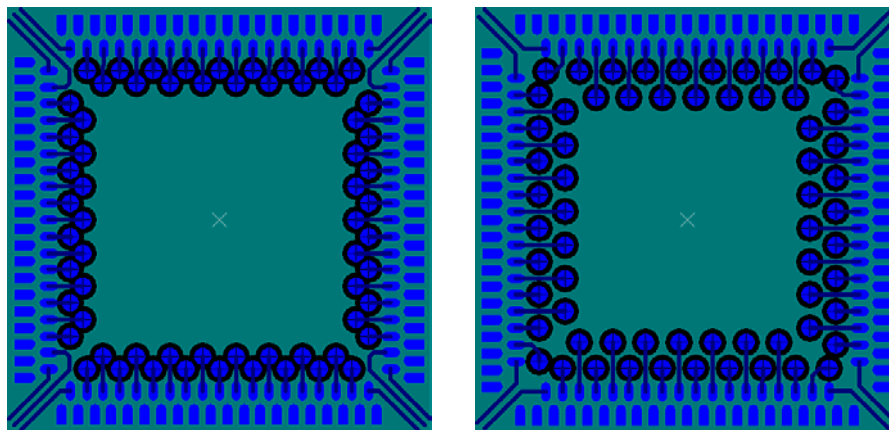


Figure 6: Land Pattern for 0.65 mm pitch Dual Row MLF.

### 3.4. Inner Row Signal Routing Considerations and Thermal Pad Size

Because of the requirement for inner row signal routing, the lead pitch of the package will determine how many layers are required for signal routing and if vias are required. The design and spacing of the vias will have an impact on internal ground plane continuity and limit the maximum size of the thermal pad. For 0.65mm pitch packages, it was previously shown in section 3.3.2 it is possible to route all signals on a single layer by routing the inner row traces between outer row leads.

For 0.50mm pitch packages, vias will be required to route inner row signals. The spacing of the vias are determined by the end application electrical and thermal requirements since via spacing impacts the internal plane layer continuity. When the vias are closely spaced, this results in 4 continuous slots in the internal plane layers due to internal anti-pads merging together. This will have an impact on electrical performance because it breaks up the ground plane. Thermal performance will also suffer as internal plane heat conduction paths are constrained to the corners between the slots. When the vias are spaced wider apart, the internal planes can be made continuous by maintaining a minimum copper web between anti-pads. This will improve electrical and thermal conduction. But the maximum thermal pad size is reduced due to increased spacing between vias. See figure 7 which shows the effect of vias spacing on internal plane layer continuity.



Narrow via spacing  
Slotted plane layer

Wide via spacing  
Continuous plane layer

**Figure 7: Via spacing effect on internal plane continuity.**

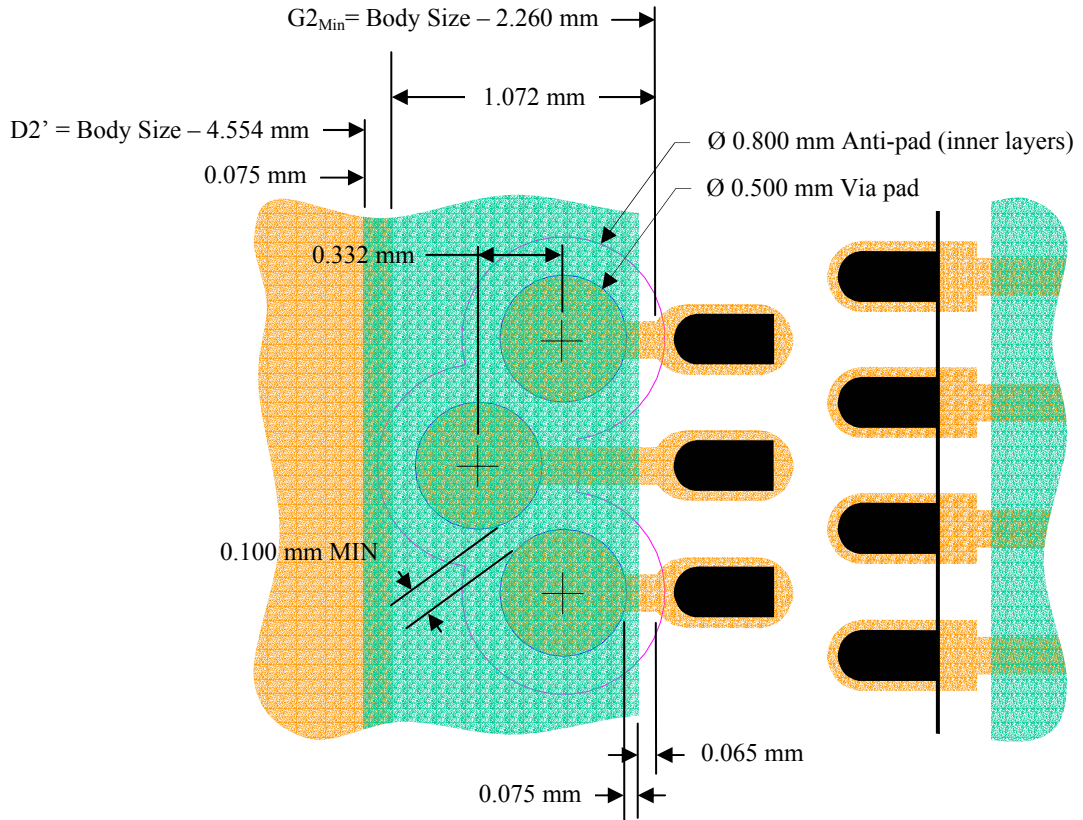
Normally, the size of the thermal pad should at least match the exposed die paddle size. But due to needed clearances for vias, the thermal pad size may need to be reduced less than the package paddle size. From a board mounting perspective, no issues have been seen when the board thermal pad is smaller than the package paddle size. Thermal pads as small as 80% of the paddle size have been mounted successfully without issue. From a thermal efficiency perspective, there is minimal impact as long as the thermal pad on the board is at least the same size as the die inside the package.

Board design rules assumptions for standard 4-layer using ½ oz Cu were made to determine via spacing requirements. The following values were used in the analysis:

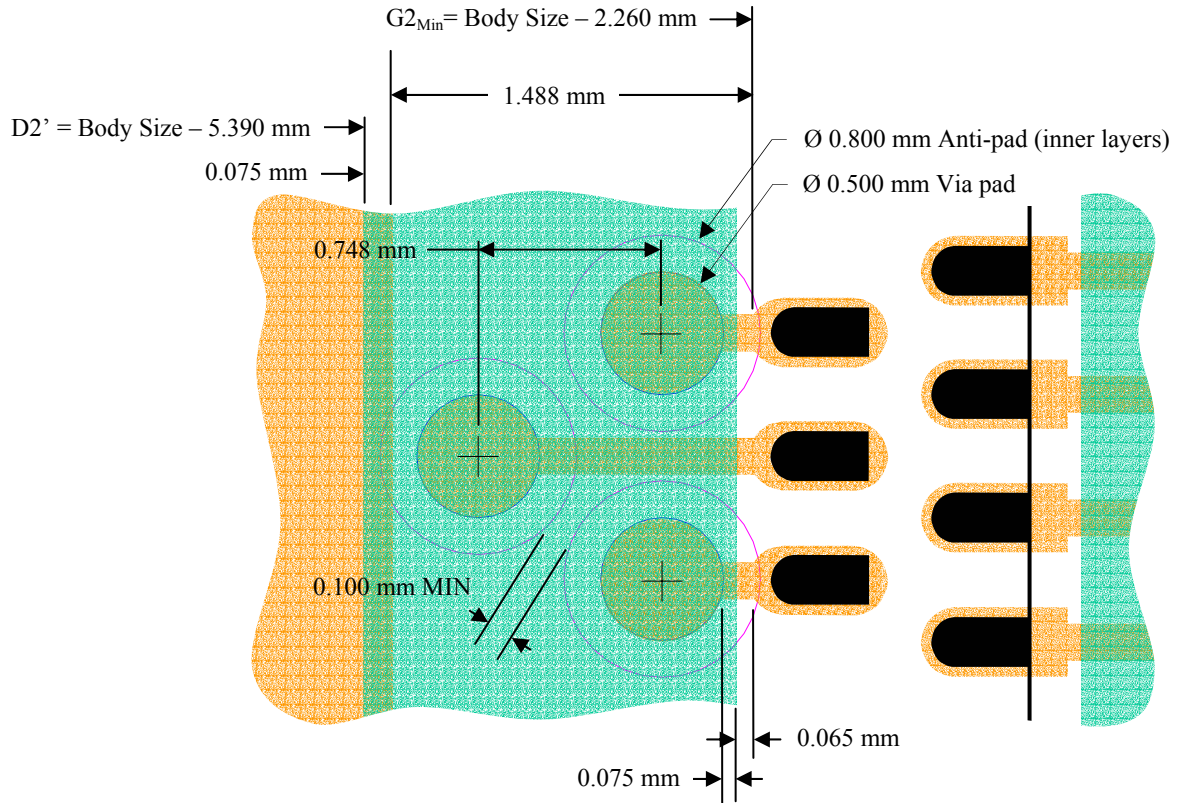
- Min Drill Diameter: 0.300 mm
- Min finished hole diameter: 0.250 mm
- Via capture pad diameter: 0.500 mm (breakout assumed per IPC-A-600, class 1,2)
- Inner layer anti-pad diameter: 0.800 mm
  
- Min outer line widths: 0.100 mm (0.125 mm preferred)
- Min outer line spacing: 0.100 mm
- Min inner line widths: 0.100 mm (0.125 mm preferred)
- Min inner line spacing: 0.100 mm
  
- Min solder mask land clearance: 0.060 mm (0.075 mm preferred)
- Min Land – trace clearance: 0.125 mm (0.150 mm preferred)
- Min solder mask feature size: 0.075 mm (0.100 mm preferred)

Figure 8 shows the resulting land pattern dimensions for the closely spaced vias on 0.500 mm pitch devices. Figure 9 shows the resulting land pattern dimensions for widely spaced vias on 0.500 mm pitch devices.





**Figure 8: 0.500mm pitch land pattern using closely spaced vias.**



**Figure 9: 0.500mm pitch land pattern using widely spaced vias.**

**Table 1: Component and PCB Land Pattern Dimensions for Full Lead and Lead Pullback Options**

Package						Package Dimensions									Board Land Pattern Dimenisons						
Size	I/O	Inner Row Leads / Side	Outer Row Leads / Side	Lead Pitch (eT)	Row Pitch (eR)	D(min)	S1(nom)	S2(nom)	S3(nom)	b(min)	b(max)	L(min)	L(nom)	L(max)	Z1(max)	G1(Min)	Z2(max)	G2(min)	X	Y1	Y2
9x9	84	9	12	0.65	0.75	8.90	8.20	7.50	6.70	0.18	0.30	0.3	0.40	0.45	9.34	8.12	7.86	6.74	0.28	0.61	0.56
9x9	108	13	14	0.50	0.65	8.90	8.20	7.70	6.90	0.18	0.30	0.3	0.40	0.45	9.34	8.12	7.86	6.74	0.28	0.61	0.56
9x9	116	13	16	0.50	0.65	8.90	8.20	7.70	6.90	0.18	0.30	0.3	0.40	0.45	9.34	8.12	7.86	6.74	0.28	0.61	0.56
10x10	100	11	14	0.65	0.75	9.90	9.20	8.50	7.70	0.18	0.30	0.3	0.40	0.45	10.34	9.12	8.86	7.74	0.28	0.61	0.56
10x10	124	15	16	0.50	0.65	9.90	9.20	8.70	7.90	0.18	0.30	0.3	0.40	0.45	10.34	9.12	8.86	7.74	0.28	0.61	0.56
10x10	132	15	18	0.50	0.65	9.90	9.20	8.70	7.90	0.18	0.30	0.3	0.40	0.45	10.34	9.12	8.86	7.74	0.28	0.61	0.56
12x12	124	12	15	0.65	0.75	11.90	11.20	10.50	9.70	0.18	0.30	0.3	0.40	0.45	12.34	11.12	10.86	9.74	0.28	0.61	0.56
12x12	156	19	20	0.50	0.65	11.90	11.20	10.70	9.90	0.18	0.30	0.3	0.40	0.45	12.34	11.12	10.86	9.74	0.28	0.61	0.56
12x12	164	19	22	0.50	0.65	11.90	11.20	10.70	9.90	0.18	0.30	0.3	0.40	0.45	12.34	11.12	10.86	9.74	0.28	0.61	0.56

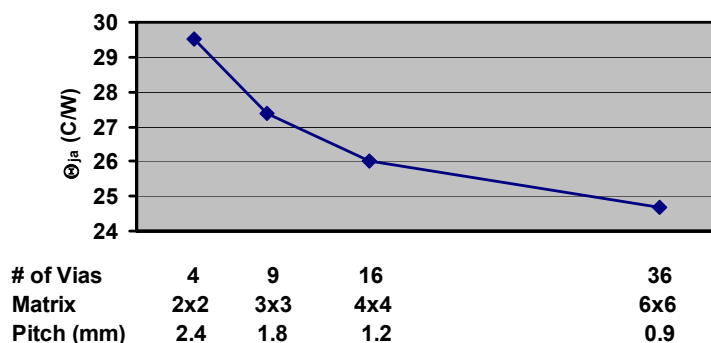
All Dimensions in mm

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### 3.5. Thermal Pad Via Design

The dual row MLF package is designed to provide the same superior thermal performance as the single row version. This requires incorporation of a thermal pad and thermal vias on the PCB. While thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die paddle on the board), thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat.

In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias need to be incorporated into the thermal pad design. Because the thermal attributes of dual row MLF are very similar to standard single row MLF, the same guidelines can be used. The number of thermal vias will depend on the application and power dissipation and electrical requirements. Although more thermal vias improve the package thermal performance, there is a point of diminishing returns as additional thermal vias may not significantly improve the performance. This is shown in Figure 10 where the effect of number of vias on  $\Theta_{ja}$  is plotted for standard 7x7 MLF 48 lead package. A via diameter of 0.3mm was used for this simulation. As the via pitch decreases more vias can be incorporated for the same thermal pad size but the incremental performance improvement goes down.



**Figure 10: Effect of Number of Thermal Via on Package Thermal Performance.**

Based on this and similar thermal simulations from standard single row MLF, it is recommended that an array of thermal vias should be incorporated at 1.0 to 1.2mm pitch with via diameter of 0.3 to 0.33 mm. For a complete discussion on via tenting, please see application notes for standard MLF package.

### 3.6. Solder Masking Considerations

Non solder mask defined (NSMD) pads are recommended for dual row applications since copper etching process has tighter control than solder masking process and improves the reliability of solder joints as solder is allowed to wrap around the sides of metal pads.

Solder mask clearance recommendations are shown in section 3.3 as part of the land pattern figures. For 0.50mm pitch applications, solder mask may be completely excluded between the leads to create a “trench” pattern. However, if desired, each land may have its own opening to create “dams” between leads. For 0.65mm pitch applications which route signals between outer row leads, individual land openings are required to prevent solder bridging to the signal traces.

For the center thermal pad, a solder mask defined (SMD) structure is recommended

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## 4. Board Mounting Guidelines

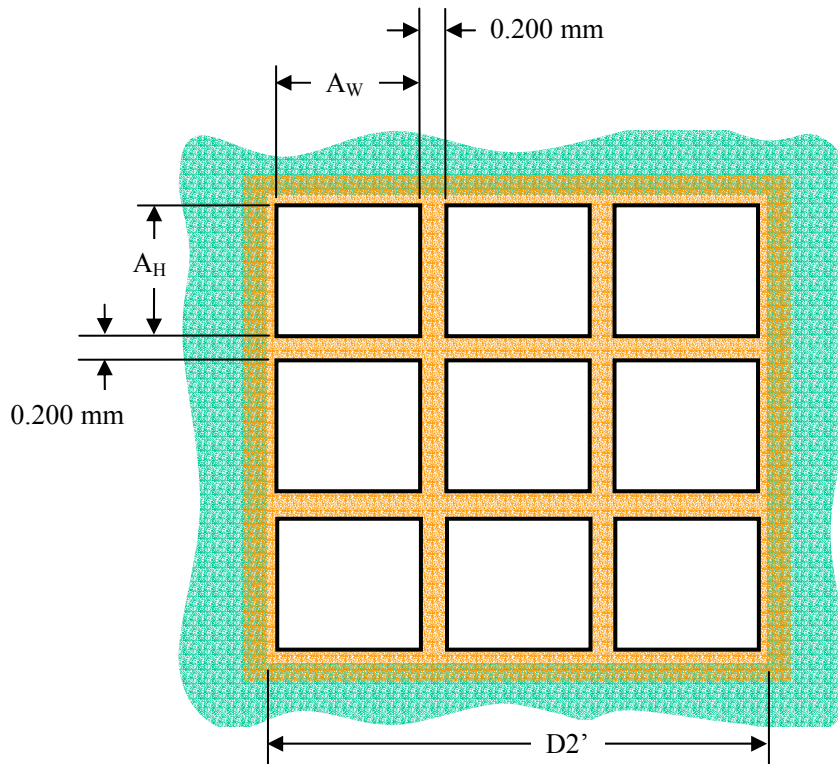
Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for dual row MLF packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Special considerations are needed in stencil design and paste printing for both perimeter leads and thermal pads. Since surface mount process varies from company to company, careful process development is recommended. The following provides some guidelines for stencil design based on Amkor's experience in surface mounting of dual row MLF packages.

### 4.1. Stencil Design for Perimeter Leads and Thermal Pad

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement. Stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled as these tolerances can effectively reduce the aperture size.

Board mounting studies on dual row MLF have found that standoff height is primarily determined by thermal pad paste coverage. The floating effects of the perimeter leads were minor and not a significant factor in determining standoff. It was also determined that not enough paste on the thermal pad could lead to inner row bridging due to the reduced standoff height. Area ratios and aspect ratios of 0.66 and 1.5, respectively, were never exceeded to maintain proper stencil design. As a result of these studies, an optimum stencil design for the land pattern described above is as follows:

- Inner row perimeter leads should be 1:1 to the land pattern (ex. Stencil aperture = Land pad = 0.28 x 0.56 mm)
- Outer row perimeter leads should be 1:1 to the land pattern (ex. Stencil aperture = Land pad = 0.28 x 0.61 mm)
- Thermal pad design should have 75% paste coverage and use a hatch pattern as shown below in figure 11. The number of openings should be chosen such that  $A_H$  and  $A_W = 1.00 \pm 0.15$ mm. Maintaining a web thickness between openings of 0.200 mm will allow space for flux volatiles to escape thus minimizing voids.



**Figure 11: Thermal Pad Stencil Designs for dual row MLF Packages**

#### 4.2. Stencil thickness and Solder Paste

The stencil thickness of 0.125mm is recommended for both 0.50mm and 0.65mm pitch dual row parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Since not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 or type 4 paste may be used for mounting MLF packages. Nitrogen purge is also recommended during reflow.

#### 4.3. Reflow Profile

Reflow profile and peak temperature has a strong influence on void formation. Amkor recommends users follow the reflow profile recommendations of the paste supplier, since this is specific to the requirements of the flux formulation.

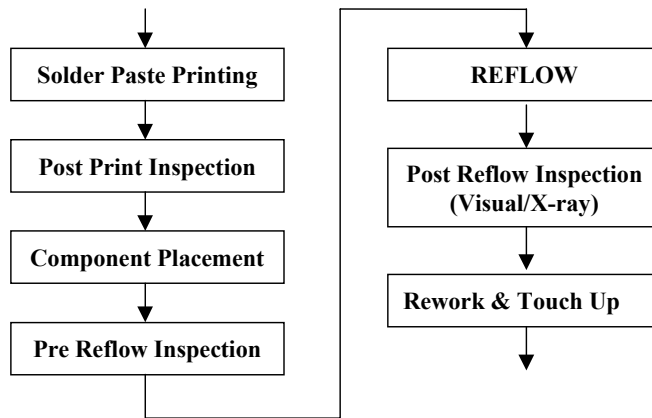
### 5. Assembly Process Flow

Figure 18 shows the typical process flow for mounting surface mount packages to printed circuit boards. The same process can be used for mounting the MLFs without any modifications. It is important to include post print and post reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted package should be inspected in transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may also be required to determine the fillet shape and size and joint standoff height.

Typical reflow profiles for No Clean solder paste are shown in Figure 16. Since the actual reflow profile depends on the solder paste being used and the board density, Amkor does not recommend a specific profile. However, the temperature should not exceed the maximum temperature the package is qualified for according to moisture sensitivity

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level. The time above liquidus temperature should be around 60 seconds and the ramp rate during preheat should be 3°C/second or lower.



**Figure 18: Typical PCB Mounting Process Flow.**

## 6. Rework Guidelines

Since solder joints are not fully exposed in the case of MLFs, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of MLF packages can be a challenge due to their small size. In most applications, MLFs will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

- Component Removal
- Site Redress
- Solder Paste Application,
- Component Placement, and
- Component Attachment.

These steps are discussed in the following in more detail. Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

### 6.1. Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause CSP to skew. Air velocity of 15 – 20 liters per minute is a good starting point.

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Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad liftoff.

## **6.2. Site Redress**

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

## **6.3. Solder Paste Printing**

Because of their small size and finer pitches, solder paste deposition for MLFs requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100X magnification. The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side also. A 125 microns thick stencil with aperture size and shape same as the package land should be used. Also, no-clean flux should be used, as small standoff of MLFs does not leave much room for cleaning.

## **6.4. Component Placement**

MLF packages are expected to have superior self-centering ability due to their small mass and the placement of this package should be similar to that of BGAs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

## **6.5. Component Attachment**

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.